CMOS Bandgap Reference and Current Reference with Simplified Start-Up Circuit

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Abstract

This paper presents a CMOS bandgap reference and current reference based on the resistor compensation. The proposed architecture consists of various high positive temperature coefficient (TC) resistors, a two-stage operational transconductance amplifier (OTA) and a simplified start-up circuit in 0.35-μm CMOS process. In the proposed bandgap reference and current reference, numerous compensated resistors, which have a high positive temperature coefficient (TC), are added to the parasitic n-p-n and p-n-p bipolar junction transistor devices, to generate a temperature-independent voltage reference and current reference. With the simplified start-up circuit, the proposed resistor-compensation bandgap reference and current reference can be started at 43 ns at a minimum supply voltage of 1.35 V. The measurements verify the current reference of 735.6 nA, the voltage reference of 888.1 mV, and the power consumption of 91.28 μW at a supply voltage of 3.3 V. The voltage TC is 49 ppm/℃ in the temperature range from 0°C to 100°C and 12.8 ppm/℃ from 30°C to 100°C. The current TC is 119.2 ppm/℃ at temperatures of 0°C to 100°C. Measurement results also demonstrate a stable voltage reference at high temperature (> 30°C), and a constant current reference at low temperature (< 70°C).

Keywords

Bandgap Reference; Current Reference; Resistor Compensation; Temperature Coefficient; Start-up Circuit

Introduction

A bandgap reference is extensively adopted in several integrated circuits, including analog, mixed-mode and memory circuits. In CMOS bandgap reference design, the sub-1-V curvature-compensated CMOS bandgap reference is favored for use with resistive subdivision methods [1-3], parasitic n-p-n and p-n-p bipolar junction transistor devices [4], and the compensation approaches associated with layout, operational amplifiers, and V_{EB} linearization [5-7]. However, the low-voltage bandgap reference frequently functions with a higher temperature coefficient than the conventional bandgap reference [4]. To reduce the temperature coefficient further, many curvature compensations have been introduced. Guan *et al.* developed a current mode curvature-compensated BGR (bandgap reference) using the trimming approach [8]. Leung *et al.* introduced second-order curvature compensation based on resistors with opposing temperature coefficients [9]. Audy introduced a third- order curvature compensation with a low-TCR resistor in parallel with a high-TCR resistor and in series with low-TCR tail resistors [10]. Malcovati had designed a high-order curvature temperature compensation method with Malcovati topology [7]. Chen also presented a programmable and high-precision temperature independent current reference by adding a positive TC current to a negative TC circuit [11]. However, the simulation result had not been verified yet.

Start-up circuits are required to prevent the bandgap reference from operating at the zero point. The components of a start-up circuit must be limited to three or less. Xing *et al.* developed a start-up circuit that comprised three NMOSs, M_{S1}-M_{S3} [5]. Xiaokang Guan *et al.* also introduced a start-up circuit with a resistor R_6 and two PMOSs, M_7-M_8 [8]. Ker further developed two start-up circuits in the proposed bandgap reference. One consists of one PMOS and two NMOSs, M_{SN1}-M_{SN3}. The other comprises a NMOS and two PMOSs, M_{SP1}-M_{SP3} [4]. Unfortunately, as is well known, the rise times of the proposed start-up circuits are long. More effort must be made to design a high-speed start-up circuit. Additionally, the current trend in industry is toward new bandgap references with simultaneous voltage reference and current reference [3], [12]. If a temperature-independent current reference is required, then the bandgap reference must generally be divided by a resistance. However, the resistance depends on temperature. Accordingly, a current reference also depends on a curvature-compensation method. This work presents a resistor-

compensation CMOS bandgap and current reference with a current reference of 735.6 nA and a voltage reference of 888.1 mV at a supply voltage of 3.3 V in a standard 0.35-μm CMOS process. The proposed bandgap and current reference, which comprises a two-stage operational transconductance amplifier (OTA) with differential NMOS input stage, is validated. Notably, the voltage TC is 49 ppm/℃ in the temperature range from 0°C to 100°C, and 12.8 ppm/℃ from 30°C to 100°C; the power consumption is 91.28 μW. Hence, section II describes the basic principles and circuit designs associated with the proposed bandgap and current reference. Section III presents and discusses experimental results. Conclusions are finally drawn in Section IV, along with recommendations for future research.

Basic Principles and Circuit Design

Basic Principles of CMOS Bandgap Reference

The temperature-independent bandgap reference is the conventionally adopted voltage reference because temperature commonly skews the operating point and affects noise in the semiconductor. A bandgap reference working with zero TC, which has both positive TC and negative TC, is therefore required. Figure 1 depicts the basic framework of a bandgap reference [13-15]. The output reference voltage, V_{ref}, is

$$V_{ref} = V_{EB} + K \cdot V_t \quad (1)$$

where K is a constant which is normally equal to 17.2 [13], V_{EB} is the voltage difference between the emitter and the base in bipolar junction transistors (BJT) and V_t is the thermal voltage. V_{EB} typically exhibits a negative-TC characteristic, while thermal voltage V_t usually has a positive TC. V_t is realized from the difference between two emitter-base voltages, ΔV_{EB}, which is proportional to the absolute temperature (PTAT). However, the output voltage of the bandgap reference suffers from variation with temperature, even when curvature-compensation is considered. To solve this problem, an improved cascading CMOS bandgap reference (BGR) with second-order curvature-compensated circuit has been presented [16]. However, it does not plot a temperature-independent current reference I_{ref}. To have both voltage reference and current reference in a temperature-independent bandgap reference, the curvature-compensated method must be further investigated.

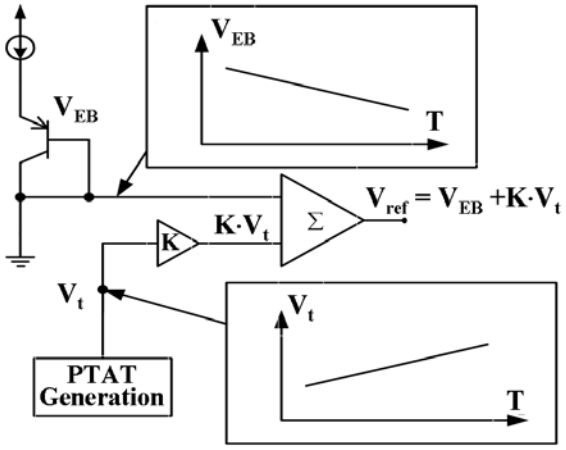


FIG. 1 BASIC FRAMEWORK FOR BANDGAP REFERENCE

Proposed Resistor Compensation Circuit

Figure 2 presents the schematic of the proposed temperature-independent bandgap reference and current reference where a two-stage operational transconductance amplifier (OTA) is used to replace a traditional cascade current mirror. Notably, Resistors, R_3 and R_{b3}, and BJT, Q_3, compensate for the output voltage reference, V_{ref}, in what is called second-order curvature compensation [9]. Resistors R_{a1} and R_{a2} have two purposes. The first is to increase the input voltages, V_{in+} and V_{in-}, of the N-type stage OTA to ensure that the OTA works properly. The second is to compensate for the temperature-dependent variation of V_{in+} and V_{in-}. The OTA is employed to equality V_{in+} and V_{in-}. Transistors Q_2 and Q_1 are vertical PNPs with a base-emitter area ratio of 5:2, passing the same current, such that the current though R_2 is PTAT. Transistors Q_1 and Q_3 are identical. R_{b1}, R_{b2} and R_{b3} are added to produce the second-order curvature compensation circuit [16]. Notably, the base-emitter area ratio of Q_2 and Q_1 is smaller than the traditional ratio, because current compensation is performed using several resistors. Therefore, the positive TCs of R_{b1}, R_{b2} and R_{b3} compensate for the negative temperature coefficients of Q_1, Q_2 and Q_3, respectively. MOSFETs M_1-M_4, are also identical to each other. They equalize the currents I_1, I_2, I_3 and I_{ref}, and provide a temperature-independent current reference I_{ref}. Restated, the proposed bandgap and current reference simultaneously provides both a temperature-independent voltage reference V_{ref} and temperature-independent current reference I_{ref}.

Next, the resistor-compensation circuit is described in detail. The emitter-base voltage V_{EB} of BJT has a negative TC whereas the emitter-base voltage difference ΔV_{BE} and all resistances have a positive TC.

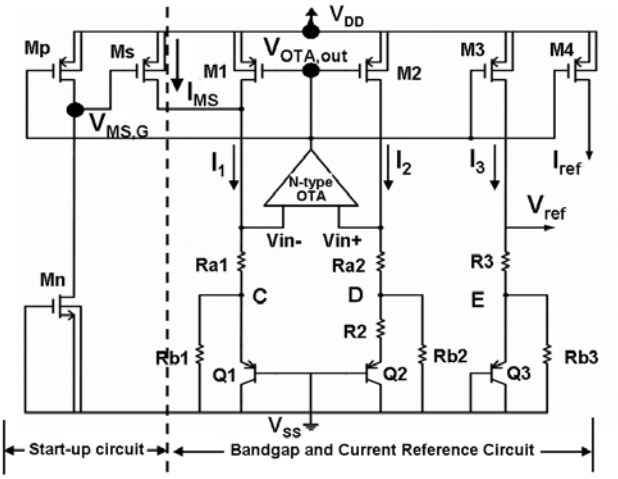


FIG. 2 SCHEMATIC OF PROPOSED RESISTOR-COMPENSATION BANDGAP AND CURRENT REFERENCE WITH VARIOUS COMPENSATED RESISTORS AND A TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

As the temperature (T) increases, the voltages, V_C, V_D and V_E, of nodes C, D and E, will drop because of the negative TC of V_{EB}; meanwhile, the values of compensated resistors, R_{b1}, R_{b2} and R_{b3}, are increased. Three compensated currents flow into the three BJTs, Q_1, Q_2, and Q_3, respectively, compensating for the emitter currents, which increase according to a positive TC such that $I_{R2} = (V_{EB1}-V_{EB2})/R_2 = \Delta V_{EB}/R_2$. This increase yields three temperature-independent currents, I_1, I_2 and I_3. Simultaneously, voltages V_{in-}, V_{in+} and V_{ref}, will be compensated for to maintain constant with resistances, R_{a1}, R_{a2} and R_3, because their TCs are positive. Hence, both voltage reference and current reference will be independent of temperature. We here need to emphasize that the compensated resistances, R_{b1}, R_{b2} and R_{b3}, must be very large and be fabricated with n-wells. However, the resistance R_2, which is fabricated with n^+-diffusion, is low and a TC of around one-third of that of n-well. Figure 3 presents the five-corner simulations of current reference I_{ref} as a function of temperature for the proposed bandgap and current reference.

The proposed resistor-compensation circuit is analyzed mathematically. For simplicity, consider components R_{a2}, R_{b2}, R_2 and Q_2 in Fig. 2. Suppose that OTA is ideal and that the counterpart resistors are equal, such that $V_{in+} = V_{in-}$, $R_{a1} = R_{a2}$ and $R_{b1} = R_{b2}$; now, $I_1 = I_2$. Therefore,

$$V_{EB1} + V_{Ra1} = V_{EB2} + V_{Ra2} + V_{R2} \quad (2)$$

$$V_{Ra1} = V_{Ra2} = I_{Ra1} \times R_{a1} = I_{Ra2} \times R_{a2} \quad (3)$$

$$I_{Ra2} = I_{Rb2} + I_{R2} = I_{Rb1} + I_{R2} \quad (4)$$

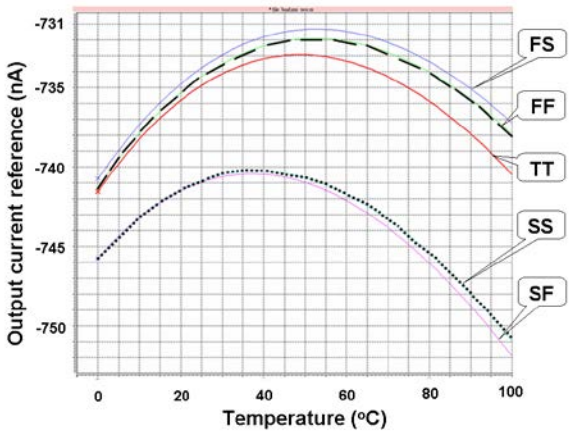


FIG. 3 OUTPUT CURRENT REFERENCE VERSUS TEMPERATURE OBTAINED BY FIVE-CORNER SIMULATIONS OF THE PROPOSED BANDGAP AND CURRENT REFERENCE

where V_{EB1} and V_{EB2} are the emitter to base voltages of the bipolar transistors, Q1 and Q2; V_{Ra1}, V_{Ra2} and V_{R2} are the voltage declines across R_{a1}, R_{a2} and R_2, and I_{Ra1}, I_{Ra2} and I_{R2} are the currents through R_{a1}, R_{a2} and R_2, respectively. Differentiating Eqn. (4) with respect to temperature (T) yields

$$\frac{\partial I_{Ra2}}{\partial T} = \frac{\partial I_{Rb2}}{\partial T} + \frac{\partial I_{R2}}{\partial T} \quad (5)$$

If a temperature-independent current reference I_{Ra2} is required, $\partial I_{Ra2}/\partial T = 0$ is set; thus,

$$\frac{\partial I_{Rb2}}{\partial T} + \frac{\partial I_{R2}}{\partial T} = 0 \quad (6)$$

where I_{Rb2} is a negative-TC current because $I_{Rb2} = I_{Rb1} = V_{EB1}/R_{b1}$, whereas I_{R2} is a positive-TC current because $I_{R2} = (V_{EB1}-V_{EB2})/R_2 = \Delta V_{EB}/R_2$. Combining the first differential item, $\partial I_{Rb2}/\partial T$ with the second differential item, $\partial I_{R2}/\partial T$, yields a temperature-independent current I_{Ra2}. Passing through the current mirror, which has MOSFETs M_1-M_4, a temperature-independent current reference I_{ref} is generated in the proposed bandgap and current reference.

The voltage reference V_{ref} associated with the bandgap and current reference can be expressed as,

$$V_{ref} = I_{R3} \times R_3 + V_{EB3} \quad (7)$$

where V_{EB3} is the emitter to base voltage of the BJT Q3 and I_{R3} is the current through resistor R_3. Notably, I_{R3} equals I_3, which is a temperature-independent current. Differentiating the above equation with respect to temperature (T) yields

$$\frac{\partial V_{ref}}{\partial T} = R_3 \times \frac{\partial I_{R3}}{\partial T} + I_{R3} \times \frac{\partial R_3}{\partial T} + \frac{\partial V_{EB3}}{\partial T} \quad (8)$$

A temperature-independent bandgap reference is obtained by setting $\partial V_{ref}/\partial T \approx 0$ and $\partial I_{R3}/\partial T \approx 0$. Therefore,

$$I_{R3} \times \frac{\partial R_3}{\partial T} + \frac{\partial V_{EB3}}{\partial T} = 0 \quad (9)$$

where R_3 is a positive-TC resistor, whereas V_{EB3} is a negative-TC voltage. Properly setting the value of R_3 yields a temperature-independent voltage reference, $\partial V_{ref}/\partial T \approx 0$. Notably, R_3 not only compensates for the temperature variation of V_{EB3}, but also adjusts the output voltage as required. Moreover, resistors R_3 and R_{b3} are fabricated using an n-well. The resistance R_3 exceeds R_{a2}, while R_{b3} is less than R_{b2}.

Figure 4 schematically depicts the complete circuit of the proposed bandgap and current reference, which simultaneously provides temperature-independent voltage reference V_{ref} and current reference I_{ref}. The left-hand side of Fig 4 presents an OTA circuit with N-type input [14], which is used to ensure that the positive input V_{in+} equals the negative input V_{in-} of OTA. Notably, the MOSFET, M_r, must be operated in the triode region as a resistor. The simulations of the two-stage telescopic OTA indicate those dc gain, bandwidth and phase margins are 61.35 dB, 9.52 MHz and 64°, respectively. If an input offset voltage of OTA, owing to asymmetries, is considered, it will introduce error in the voltage reference V_{ref} . Thus,

$$V_{ref} = V_{EB3} + \left(\frac{R_3}{R_2}\right)\left(V_T \times \ln m - V_{OS}\right) + I_{Rb2}R_3 \quad (10)$$

where V_{OS} is the input offset voltage of OTA, V_T is the thermal voltage, and m is the base-emitter area ratio of Q2 to Q1, producing $m \approx 5/2$. In this work, two methods are employed to lower the effect of V_{OS}. One is that the OTA is a telescopic topology to minimize the offset because of symmetry and the other is that the layout of OTA incorporates common centroid and dummy in a large device.

Proposed Start-up Circuit

As shown in Fig. 2, the start-up circuit comprises three MOSFETs, M_n, M_P and M_S, where the gate-source voltage V_{GS}, of M_n is shorted to turn off M_n with a huge resistance. Restated, the gate voltage of M_S, $V_{MS,G}$, is half of the supply voltage V_{DD} in the initial stage because both M_P and M_n are cut-off. As the supply voltage V_{DD} increases slowly, $V_{OTA,out}$, which is connected to the gate terminal of M_P, traces V_{DD} because the OTA is off and the voltage difference between source (V_{DD}) and gate of M_P is about zero due to the C_{gs} of M_P, M_1 and M_2. When M_S is turned on under the condition V_{DD}-$V_{MS,G} \geq |V_{thp}|$ with a threshold voltage of PMOS, $|V_{thp}|$, a small conduction current I_{MS} flows. Then the conduction resistance between drain and source, r_{DS}, of M_P is reduced. By comparing with the huge resistance of M_n, the gate voltage of M_S increases. M_P flows current until V_{DS} is reduced to nearly 0 V. The voltage of $V_{MS,G}$ keeps V_{DD} due to parasitic capacitance.

Finally, the operation mode of Mp is changed from saturation to the linear region and M_S will be turned off. Note that the M_n is used not only to speed-up the rise time, but also to save power without driving current. Figure 5 plots the simulated results concerning the start-up circuit over time, where the symbols ▲, ■, ★ and ◆ represent the power-supply voltage (V_{DD}), the gate voltage of M_S ($V_{MS,G}$), the output voltage of OTA ($V_{OTA,out}$) and the source current of Ms (I_{MS}), respectively. Importantly, the minimum power supply, $V_{DD,min,}$ is approximately 1.35 V, and the difference between the power-supply voltage (V_{DD}) and the gate voltage of M_S ($V_{MS,G}$), $V_{DD} - V_{MS,G}$, exceeds 0.7 V; the start time is around 43 ns, and the source current of M_S, I_{MS}, falls to zero.

Experimental Results

The proposed bandgap and current reference was fabricated with 0.35-μm 2P4M CMOS process. The layout is carefully considered to minimize the mismatches of the resistor and that of the transistor. Additionally, resistors R_{a1} and R_{a2} are implemented using n-well because of its large temperature coefficient, while n+-diffusion occurs in resistor R_2 with a small temperature coefficient. The temperature-dependent performance was measured over operating temperatures from 0°C to 100°C. Figures 6 and 7 plot the measured voltage reference V_{ref} and current reference I_{ref}, respectively, of the proposed bandgap and current reference against temperature. Figure 6 indicates that the measured voltage reference is proportional to the temperature in the range 0°C to 30°C, and is roughly constant from 30°C to 100°C. The temperature coefficient of the voltage reference is approximately 49 ppm/°C and the maximum variation of V_{ref} is approximately 4.35 mV at a supply voltage of 3.3 V and temperatures from 0°C to 100°C. The corresponding values are 12.8 ppm/°C and 0.8 mV from 30°C to 100°C. Figure 7 reveals that the measured current reference is almost constant from 0°C to 70°C, but increases rapidly in

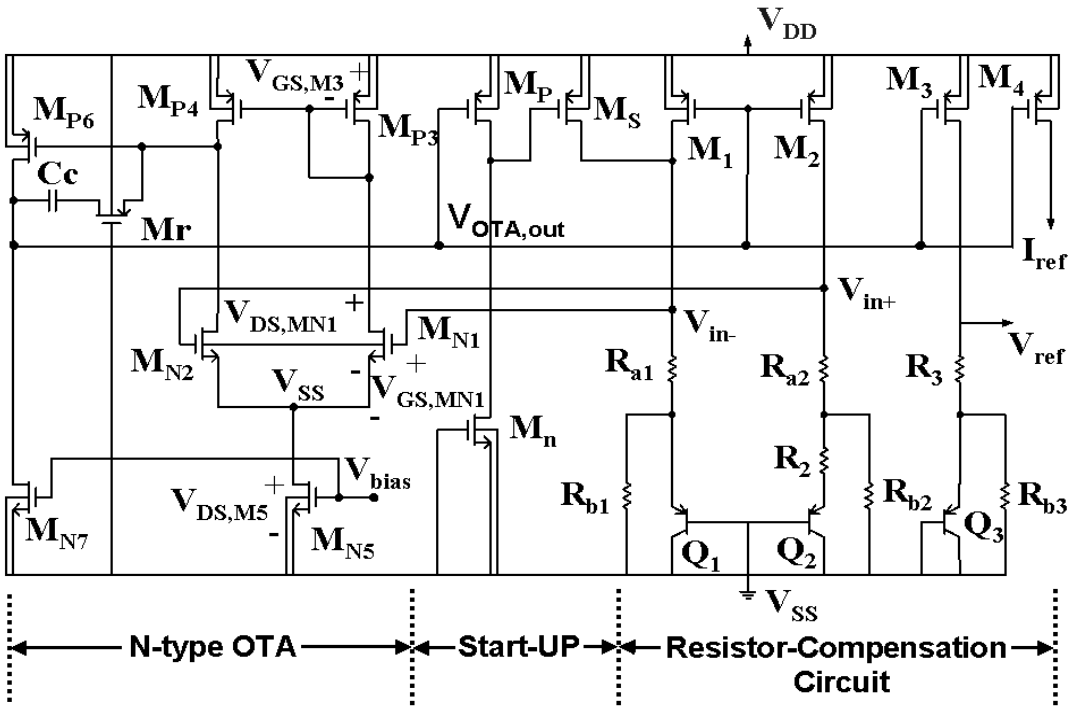
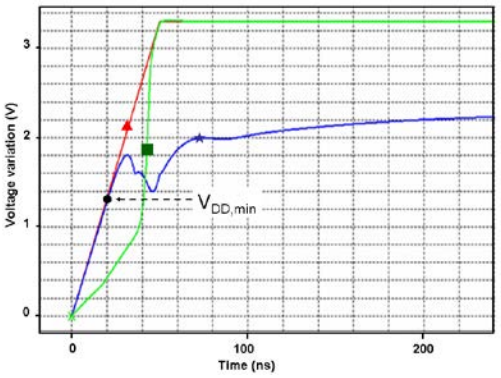


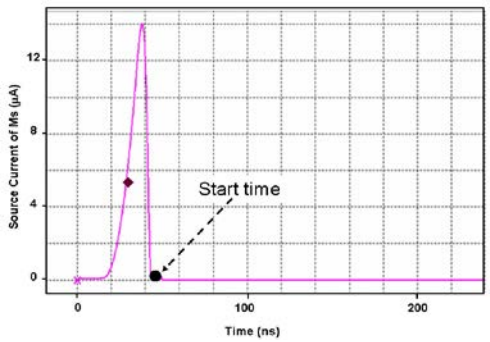
FIG. 4 COMPLETE CIRCUIT OF THE PROPOSED BANDGAP AND CURRENT REFERENCE WHICH SIMULTANEOUSLY PROVIDES TEMPERATURE-INDEPENDENT VOLTAGE REFERENCE AND CURRENT REFERENCE

temperature range 70°C to 100°C. The temperature coefficient of the current reference is about 119.3 ppm/°C and the maximum variation of I_{ref} is about 8.77 nA at temperatures from 0°C to 100°C. Additionally, the variations in voltage reference are measured, and plotted in Fig. 8 versus the power supply voltage from 0 V to 3.6 V. The measurements also demonstrate that output voltages from 0.871 V to 0.888 V are roughly proportional to the power supplied from 1.4 V to 3.4 V. Notably, the proposed bandgap and current reference can be started up at a supply voltage of 1.35 V, and so is suitable for operating with battery cell.

Table I presents the measurements of the proposed bandgap and current reference. Table II compares the proposed resistror-compensation bandgap and current reference presented herein with other prior-art curvature-compensation bandgap references. In table II, the best voltage TC of 12.8 ppm/℃ is superior to that of other bandgap references, except [5], and the best current TC of 119.2 ppm/℃ is acceptable by comparing with reference [19]. Based on the comparison, the proposed bandgap and current reference is suitable for use at temperatures of over 30°C. However, the averaged current reference is lower. Note that large compensated resistors, R_{b1}, R_{b2} and R_{b3}, were selected herein to reduce power consumption of



(a)



(b)

FIG. 5 SIMULATED RESULTS CONCERNING START-UP CIRCUIT OVER TIME IN NS. (A) VARIATIONS OF V_{DD} (▲), $V_{MS,G}$ (■) AND $V_{OPA,OUT}$(★) IN VOLT (V). (B) SOURCE CURRENT OF MS (◆) IN MICRO AMPERES (μA)

the chip and high positive-TC resistors, R_{a1} and R_{a2}, were adopted to compensate for the temperature-dependent variation of V_{in+} and V_{in-} in OTA. Figure 9 presents a die microphotograph of the proposed bandgap and current reference fabricated in a 0.35-μm CMOS process. In this chip, two capacitors, C1 and C2, are connected to power supply and voltage reference, respectively, to alleviate the unstableness.

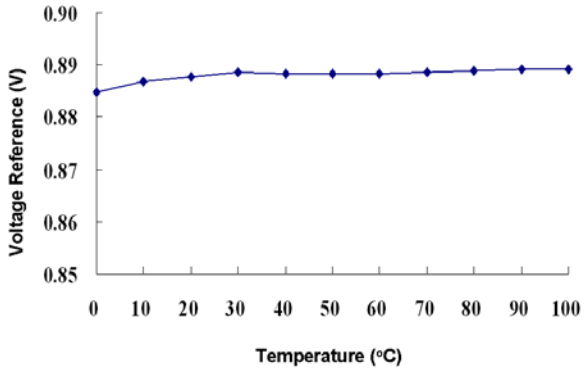


FIG. 6 MEASURED VOLTAGE REFERENCE (V) AS A FUNCTION OF TEMPERATURE (°C)

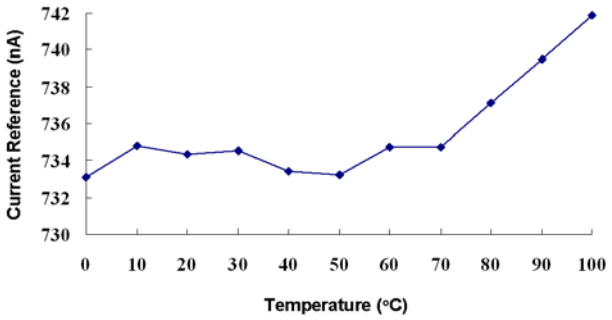


FIG. 7 MEASURED CURRENT REFERENCE (NA) AS A FUNCTION OF TEMPERATURE (°C)

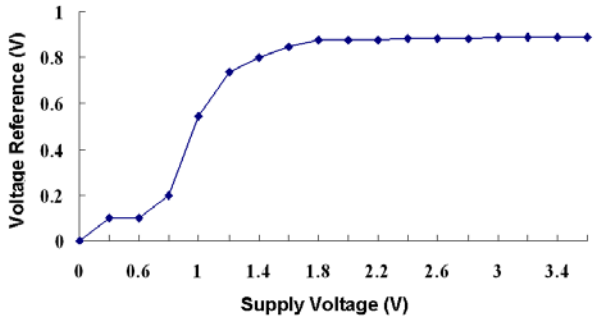


FIG. 8 VARIATION OF OUTPUT REFERENCE VOLTAGE (V) AGAINST SUPPLY VOLTAGE (V) FOR THE PROPOSED BANDGAP AND CURRENT REFERENCE

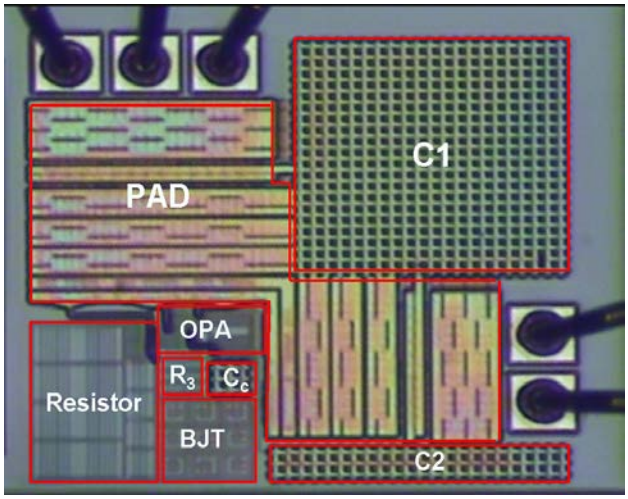


FIG. 9 DIE MICROPHOTOGRAPH OF THE PROPOSED BANDGAP REFERENCE AND CURRENT REFERENCE FABRICATED IN A 0.35-μM CMOS PROCESS

TABLE I MEASUREMENTS OF PROPOSED BANDGAP REFERENCE AND CURRENT REFERENCE

Parameters	Measurements
Typical power supply (V)	3.3
Minimum power supply (V)	1.35
Averaged voltage reference (mV) (0℃~100℃)	888.1
Maximum variation of voltage reference (mV) (0℃~100℃)	4.35
Voltage temperature coefficient (ppm/℃) (0℃~100℃)	49
Averaged voltage reference (mV) (30℃~100℃)	888.7
Maximum variation of voltage reference (mV)(30℃~100℃)	0.8
Voltage temperature coefficient (ppm/℃) (30℃~100℃)	12.8
Voltage reference settling time (V/μs)	38.1
Averaged current reference (nA) (0℃~100℃)	735.6
Maximum variation of current reference (nA) (0℃~100℃)	8.77
Current temperature coefficient (ppm/℃) (0℃~100℃)	119.2
Power dissipation (μW)	91.28
Chip area (μm×μm)	237×256

Conclusions

A resistor-compensation CMOS bandgap reference and current reference with a current reference of 735.6 nA and a voltage reference of 888.1 mV at a supply voltage of 3.3 V was presented. It consumes a maximum power of 91.28 μW. The voltage TC was 49

TABLE 2 COMPARISON AMONG THE CURVATURE-COMPENSATED BANDGAP REFERENCES

	This work	**[17]**	**[18]**	**[19]**	**[5]**	**[3]**
Technology	0.35 μm	0.35 μm	0.25 μm	0.18 μm	0.18 μm	0.13 μm
Typical V_{DD} (V)	3.3	3.3	NA	1.0	1.1	1.2
Minimum V_{DD} (V)	1.35	NA	0.85	NA	0.90	NA
Averaged voltage reference (0℃~100℃)	888.1 mV	1173.2 mV	238.2 mV	598.5 mV	657 mV	630 mV
Voltage TC (0℃~100℃)	49 ppm/℃	47 ppm/℃ (trimming)	58 ppm/℃	125 ppm/℃	10 ~ 40 ppm/℃	29 ppm/℃
Voltage TC (30℃~100℃)	12.8 ppm/℃					
Averaged current reference(nA) (0℃~100℃)	735.6 nA	NA	NA	144 μA	NA	50.2 μA
Current TC (0℃~100℃)	119 ppm/℃	NA	NA	185 ppm/℃	NA	18 ppm/℃
Temperature Range	0~100℃	-75~75℃	-10~120℃	0~100℃	0~150℃	-10~100℃

ppm/℃ at temperatures from 0°C to 100°C, and 12.8 ppm/℃ from 30°C to 100°C. The current TC was 119.2 ppm/℃ from 0°C to 100°C. The measurements also reveal that a good temperature-independent voltage reference V_{ref} is realized at high temperature and a fine temperature-independent current reference I_{ref} is performed at low temperature. With a simplified start-up circuit, the proposed bandgap and current reference was verified to be effective in a standard 0.35-μm CMOS process. Restated, the proposed resistor-compensation CMOS bandgap and current reference, which is compensated with various high positive TC resistors, simultaneously provides both a temperature-independent voltage reference V_{ref} and temperature-independent current reference I_{ref}. Furthermore, this work verifies that both n-well and n+-diffusion are suitable for developing a new resistor-compensation technique in bandgap reference or current reference. To further improve the performance of bandgap reference or current reference, the resistor-compensation technique can be utilized except high-order curvature compensation [5].

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